



DIGITAL TO ANALOG CONVERTER (DAC)

USER'S MANUAL



泉 ≡ SPRING3

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OVERVIEW

Spring3

A new generation DAC of fully discrete resistor network (commonly known as R2R). Relative to its predecessor the "Spring 2" , the following improvements have been applied.

FEATURES

- ◆ A new generation of linear compensation technology. It's a better solution to the resistance and accuracy errors caused by the switching components and the PCB. After compensations have been applied, the equivalent accuracy will be 0.00005%.
- ◆ The new generation of de-glitch technology can provide a full range without increasing the noise floor or other adverse effects.
- ◆ Based on this new generation of technology, “泉3” Spring3 can provide a SINAD of >112dB and a dynamic range of >128dB, which represents the performance limit reached by today's most advanced R2R architecture DAC.
- ◆ Using the ultimate performance of PLL+FIFO technology, which provides 0.1Hz Third-Order low-pass ability to inhibit jitter. It also uses a high-performance femto-second VCXO as the PLL clock source. Under the premise of being almost immune to the front-end jitter, it can also lock up to 1.5us-2us @ 1KHz signal with high jitter.
- ◆ The USB interface uses proprietary firmware with ultra-low latency, a highly reliable data transmission, and ideal USB eye pattern measurements that contributes to 2-4 times higher performance than official firmware.
- ◆ A single, independent HDMI-I2S input interface is provided, which has a four-way independent circuit, as opposed to standard LVDS chip, making I2S clock signals subject to lower interference and lower jitter. In addition, the I2S input can be configured with a specific pinout configuration, making it compatible with most of the HDMI-I2S digital devices on the market.
- ◆ Optional (Factory installed only): A fully balanced, fully discrete analog pre-amplifier. Provides 84 steps, each step is 1db of volume control.



SPECIFICATIONS

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DIGITAL INPUT

COAXIAL1, COAXIAL2, OPTICAL, AES	PCM 44.1-192K (24bit)
	DSD 64X (DOP)
USB	PCM 44.1K-1.536M (32bit)
	DSD 64-512X (DOP)
	DSD 64-1024X (Native)
I ² S	PCM 44.1K-1.536M (32bit)
	DSD 64-1024X

ANALOG OUTPUT

PCM 48K NOS	THD+N 0.00032% @1K(-110dB)
	DNR 127dB
	DAC Voltage Output 2.9Vrms (RCA), 5.8Vrms (XLR)
	(Optional) Pre-amplifier Voltage Output 5.8Vrms (RCA), 11.6Vrms (XLR)
DSD 128X	THD+N 0.00035% @1K(-109dB)
	DNR 115dB
	DAC Voltage Output 1.45Vrms (RCA), 2.9Vrms (XLR)
	(Optional) Pre-amplifier Voltage Output 2.9Vrms (RCA), 5.8Vrms (XLR)

PHYSICAL CHARACTERISTICS

Size (Chassis)	430x300x55mm (W x L x H, Dimensions do not include protruding parts)
Weight	8.5kg



POWER SPECIFICATIONS

Power Input (configurable, see label on bottom of unit for specified input)

220-230V 50/60Hz – Fuse Type 2A SB 5x20mm

110-115V 50/60Hz – Fuse Type 4A SB 5x20mm

Power Consumption

40W



ACCESSORIES

Included Accessories

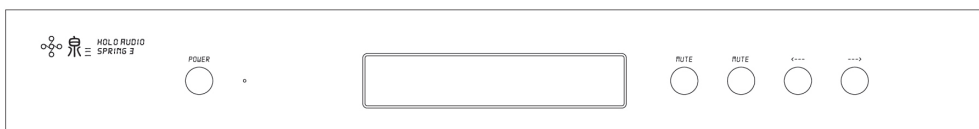
AC Power Cable x1

USB Cable x1

Remote Control x1 (Not included in Level 1 models)



FRONT PANEL



 **BUTTON CONFIGURATION**

POWER, MUTE, MENU, ← / Volume -, → / Volume +

Left of display

POWER (INDICATION LIGHT IS RED WHEN POWERED IN OFF-STATE, AND GREEN WHEN ON)

Press and hold this button for 1 second to switch the power on and off. In the off state, all is power is off except for the standby circuit and red indication light, other circuits of the Spring 3 "泉3" will stop working and stop outputting.

Right of display, 4 buttons from left to right

MUTE

In the silent mode, some of the Spring 3 "泉3" output stage circuit turns off. However, the power consumption is essentially unchanged, and will maintain its hot machine state.

MENU

In normal operation mode press this button to select the digital input (Source) mode, use the arrow buttons, ← and → to select USB (ground isolation), 12S, RCA, BNC, AES, and fiber optic.

In display mode (Display), use the arrow keys ← and → to select whether to turn off the display (Display Off) automatically; in configuration (Menu) mode, press this button to select the configuration item.

← / VOLUME -

In configuration mode, press this key to change the configuration items. (Volume - only applies when pre-amp module installed.) In the normal mode, press this key to decrease the output volume.

→ / Volume +

In configuration mode, press this key to change the configuration items. (Volume + only applies when pre-amp module installed.) In the normal mode, press this key to increase the output volume.



CONFIGURATION MODE

How to enter Configuration mode:

In shutdown mode (powered off state, red light indicated) press and hold the menu button and power button to enter menu mode. Then press the menu button to select the configuration mode, press the left button or right button to change the configuration mode.

CONFIGURATION MODE OPTIONS (LEFT TO RIGHT SELECTION)

I2S FAT

Select from HOLO, ALT1, ALT2, ALT3. Reference I2S Port Pinout for an explanation and the I2S line sequence. (See page 08)

OUT POL

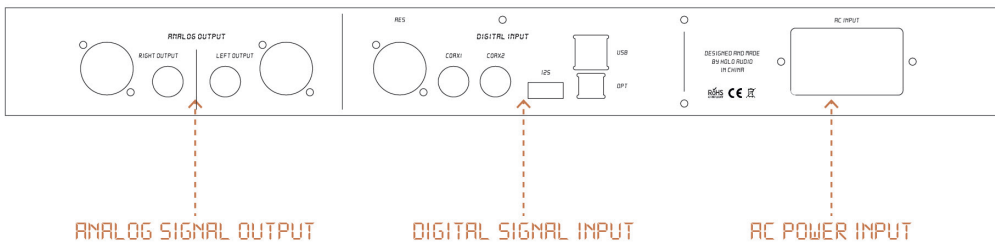
STANDARD, the analog RCA output is normal polarity, balanced XLR output 1-Ground, 2-Hot, 3-cold. REVERSED, the analog RCA output is reverse polarity, balanced XLR output 1-Ground, 2-Cold, 3-Hot.

PLL

Select ON to turn on the PLL function and work with all digital input signals to eliminate jitter. Select OFF to turn off the PLL function.

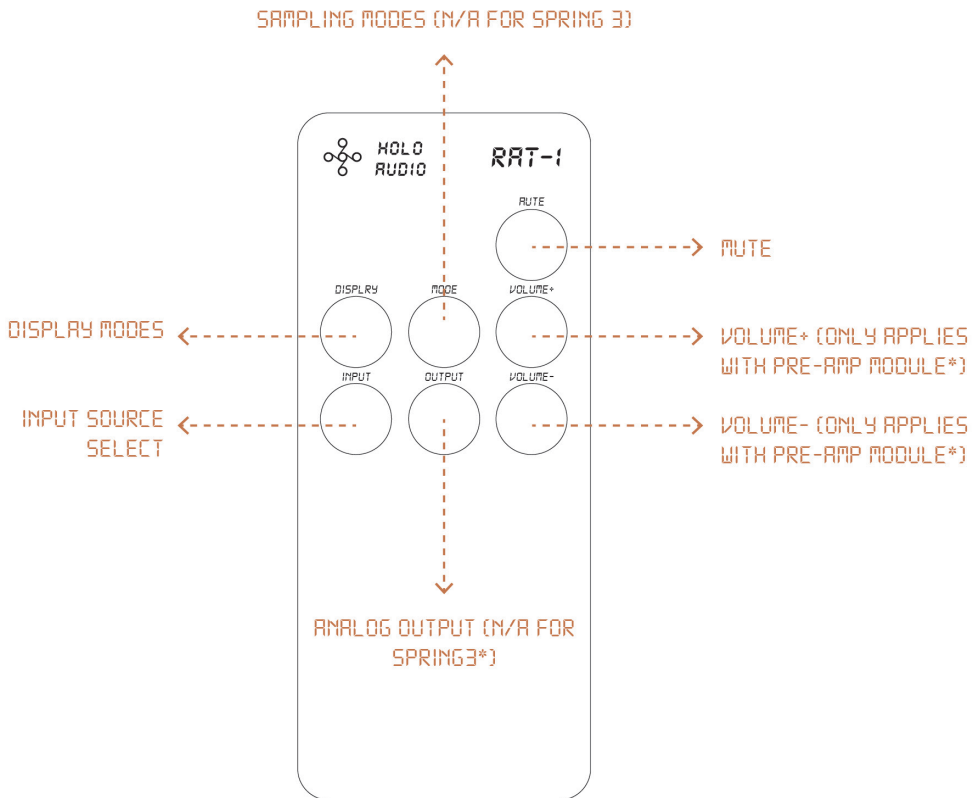


REAR PANEL





REMOTE CONTROL

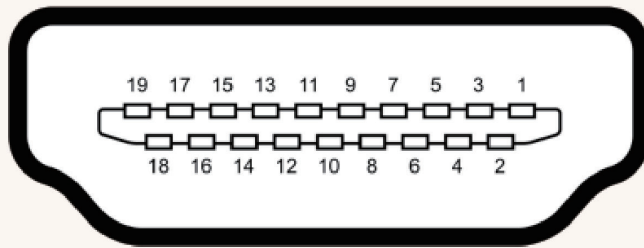


This remote control is a universal remote control for HOLO AUDIO. The sampling mode setting, and analog output setting buttons are invalid for the “泉3” Spring 3; the volume (+/-) button is only available for configuration with preamplifier. This remote will work simultaneously with other HOLO Audio branded products i.e. DACS, pre-amps and head-amps.



I2S PORT PINOUT

Using LVDS differential transmission. Physical interface and HDMI consistent, you can use the HDMI cable. But note that the electrical signal transmission is I2S, not conventional HDMI audio and video signals.



Pin	HOLO		ALT1		ALT2		ALT3	
	PCM	DSD	PCM	DSD	PCM	DSD	PCM	DSD
1	I2S_DATA-	DSD_L-	I2S_DATA+	DSD_L+	I2S_DATA-	DSD_R-	I2S_DATA+	DSD_R+
2	GND	GND	GND	GND	GND	GND	GND	GND
3	I2S_DATA+	DSD_L+	I2S_DATA-	DSD_L-	I2S_DATA+	DSD_R+	I2S_DATA-	DSD_R-
4	I2S_BCLK+	DSD_BCLK+	I2S_BCLK+	DSD_BCLK+	I2S_BCLK+	DSD_BCLK+	I2S_BCLK+	DSD_BCLK+
5	GND	GND	GND	GND	GND	GND	GND	GND
6	I2S_BCLK-	DSD_BCLK-	I2S_BCLK-	DSD_BCLK-	I2S_BCLK-	DSD_BCLK-	I2S_BCLK-	DSD_BCLK-
7	I2S_LRCK-	DSD_R-	I2S_LRCK+	DSD_R+	I2S_LRCK-	DSD_L-	I2S_LRCK+	DSD_L+
8	GND	GND	GND	GND	GND	GND	GND	GND
9	I2S_LRCK+	DSD_R+	I2S_LRCK-	DSD_R-	I2S_LRCK+	DSD_L+	I2S_LRCK-	DSD_L-
10	I2S_MCLK+	DSD_MCLK+	I2S_MCLK+	DSD_MCLK+	I2S_MCLK+	DSD_MCLK+	I2S_MCLK+	DSD_MCLK+
11	GND	GND	GND	GND	GND	GND	GND	GND
12	I2S_MCLK-	DSD_MCLK-	I2S_MCLK-	DSD_MCLK-	I2S_MCLK-	DSD_MCLK-	I2S_MCLK-	DSD_MCLK-
13	NC	NC	NC	NC	NC	NC	NC	NC
14	NC	NC	NC	NC	NC	NC	NC	NC
15	NC	NC	NC	NC	NC	NC	NC	NC
16	RSV	RSV	NC	NC	NC	NC	NC	NC
17	GND	GND	GND	GND	GND	GND	GND	GND
18	NC	NC	NC	NC	NC	NC	NC	NC
19	GND	GND	GND	GND	GND	GND	GND	GND

